DETAILED ACTION

1. Claims 15-23 have been presented for examination.

Claims 1-14 have been cancelled.

Claims 15-23 are newly presented.

PRIORITY

2. Acknowledgment is made of applicant's claim for foreign priority based on PCT/FR05/00529 filed 7 March 2005 which claims benefit from foreign application FR 0402419 filed 8 March 2004. The Examiner notes the copy of the PCT application, however, applicant has not filed a certified copy of the FR 0402419 application as required by 35 U.S.C. 119(b). See Section 5.i below.

Oath/Declaration

3. Acknowledgment is made of applicant's declaration filed 15 May 2008.

Drawings

4. Acknowledgment is made of applicant's drawings including Figures 1-18 filed 10 July 2006.

Response to Arguments

5. Applicant's arguments filed 11 March 2011 have been fully considered but they are not persuasive.

NON-PRIOR ART ARGUMENTS

i) Applicants argue that a certified copy of the foreign priority is not required where a National State application is filed. However the Examiner notes as per MPEP 1893.03(b) (II) that the foreign priority document is required. The Examiner further notes that the office has not received a certified copy of the foreign priority document, nor has one been forwarded from the International Bureau. Therefore the priority objection is **MAINTAINED.**

PRIOR ART ARGUMENTS

ii) Applicants argue that the reference does not teach a single clock that provides "representative signals of time units." However the Examiner notes that paragraph 160 of the reference recites circuit timing which is clocked according to its most precise and accurate representation of the simulation. This reads on a single clock which provides representative signals of time units. Therefore the prior art rejection is **MAINTAINED.**

iii) Applicants argue that the reference does not teach synchronous programmable logic array that processes values relative to the time units. The Examiner notes that paragraph 98 of the reference recites the system controls the global synchronization time of the processing elements which reads on the synchronous programmable logic array that processes values relative to the time units. Applicants further argue that the reference does not teach a scheduled times processor cooperative with said logic array so as to provide representative scheduled time signals according to signals of said state change detector or by said signal programmer of the event and by the signals of said clock. However the reference recites in paragraph 36 the use of a scheduler which accepts all future events and then sorts the events to be processed as scheduled events whereby the simulator tracks the simulation time and sends pending events based on the scheduling. Therefore the prior art rejection is **MAINTAINED.**

iv) Applicants argue that the reference does not teach a logic array providing a simulator operation. Paragraph 102 of the reference recites the use of hardware simulation and paragraph 61 further recites structure within the system being simulated where the structure represents changes in the states of a logic device. Applicants further argue that the reference does not teach that the time unit is tuned for a representation of the simulator operation. However as cited previously the reference recites in paragraph 36 the use of a scheduler which accepts all future events and then sorts the events to be processed as scheduled events whereby the simulator tracks the simulation time and sends pending events based on the scheduling. Paragraph 42 further recites reciting clock cycle access to data for the simulation. This reads on the limitation as presented. The Examiner notes that Applicants have merely stated the reference does not teach and has not provided support for their assertion. Therefore the prior art rejection is **MAINTAINED.**

v) Applicants argue that the reference does not teach a logic array emulating at realtime a logic function without logic emulation. The Examiner notes that Applicants have merely stated the reference does not teach and has not provided support for their assertion. As cited previously by the Examiner paragraph 25 of Hoare which shows that the invention can run at various speeds and even up to faster than real time which reads on this limitation. Paragraph 19 further recites, whereby the functional logic simulation is broken up into two parts, the logic based and the timing based. The timing propagation simulation represents non-logic element emulation. Therefore the prior art rejection is **MAINTAINED.**

vi) Applicants argue that the reference does not teach the limitations of claim 19. The Examiner notes that Applicants have merely stated the reference does not teach and has not provided support for their assertion. As cited previously by the Examiner Figure 1, element 107 whereby each simulation engine module, communicates through its single line group. Further paragraph 42 recites single clock cycle access to a block of stored data as well as the scheduler, element 110, represents the scheduled time processing unit and host workstation of Figure 1 providing a user interface for interaction. The simulation engines, elements 105, deal with the signaling for the events. The command group is represented by the scheduler which allocates events as required by timing. Therefore the prior art rejection is **MAINTAINED.**

vii) Applicants argue that the reference does not teach the limitations of claim 20. The Examiner notes that Applicants have merely stated the reference does not teach and has not provided support for their assertion. As cited previously Paragraph 42, recites single clock cycle access to a block of data and its corresponding command, such as read/write, which reads on the logic word per time unit whereby logic words are represented as read/write or other events. This is further stated in paragraph 85 whereby a read/write operation is performed in either a single clock cycle or multiple clock cycles depending on the size of the operation and its corresponding data. Therefore the prior art rejection is **MAINTAINED.**

viii) Applicants argue that the reference does not teach the limitations of claim 21. The Examiner notes that Applicants have merely stated the reference does not teach and has not provided support for their assertion. As cited previously Paragraph 37 recites that the simulation engine allows for multiple pending events, such as read/writes, to be evaluated within one or more clock cycles. Paragraph 16 recites the storage of data as it is being evaluated for scheduling which reads on the memorizing of a merged logic word in that multiple operations are performed in a single cycle and the operations are based on the scheduler "memorizing" by storing the appropriate event and its relevant data. Therefore the prior art rejection is **MAINTAINED.**

ix) The Examiner acknowledges Applicants amendments to the claims in order to avoid invocation of the 112 6th paragraph.

Claim Objections

6. **Claim 21 is objected** to because of the following informalities: The claim recites "serval respective identities." It appears Applicants intend to state "several respective identities" and the Examiner will proceed under that assumption.

Appropriate correction is required.

Claim Interpretation

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. **Claims 15-23 are rendered statutory** by virtue of their recitation of a hardware electronic circuit as well as a corresponding hardware programmable logic array, according to paragraph 14 of the specification of the instant application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 15-23 are rejected** under 35 U.S.C. 102(b) as being clearly anticipated by **Hoare, II et al. "Discrete Event Simulator" U.S. Patent Pub. No 2002/0133325, hereafter referred to as Hoare.**

Regarding claim 15:

The reference discloses A data processing circuit that emulates a logic function, the data processing circuit comprising:

a single clock providing representative signals of time units; **(Hoare. Paragraph 160, whereby the circuit timing is clocked according to its most precise and accurate representation of the simulation)**

a synchronous programmable logic array that processes values relative to the time units; **(Hoare. Paragraph 160, whereby each circuit module which represents a circuit gate or circuit subsection synchronizes based on delays required by the circuit components. Also paragraph 98 recites that the system controls the global synchronization time of the processing elements. See also paragraph 80 reciting the use of PLDs and FPGAs to emulate circuit behavior)**

a state change detector designating events of internal values or external values: **(Hoare. Paragraph 43 recites that the system monitors model state/value changes. The system further defines events as future or pending events which represent the internal or external events recited since the future/pending events are defined as those that are currently being simulated, interpreted as internal, and those that must be scheduled and then processed, interpreted as external)**

a signal programmer cooperative with said state change detector so as to change the state or the events; **(Hoare. Paragraph 86 whereby a change in one or more input signals is defined as an event which is then evaluated)** and

a scheduled times processor cooperative with said logic array so as to provide representative scheduled time signals according to signals of said state change detector or by said signal programmer of the event and by the signals of said clock, said scheduled times processor adapted to determine scheduled times at time delayed by said signal programmer, the processed values from said logic array being a result of successive scheduled times initiated by the internal values or the external values of said state change detector and by successive scheduled time determination by the scheduled times processor. **(Hoare. Paragraph 160, whereby each circuit module which represents a circuit gate or circuit subsection synchronizes based on delays required by the circuit components. Further paragraph 36 recites the use of a scheduler which accepts all future events and then**

sorts the events to be processed as scheduled events. Paragraph 36, whereby the simulator tracks the simulation time and sends pending events based on the scheduling)

Regarding claim 16:

The reference discloses The data processing circuit of Claim 15, said logic array providing a simulator operation, **(Hoare. Paragraph 102 reciting hardware simulators)** the time unit being tuned for a reproduction of the simulator operation. **(Hoare. Paragraph 42, reciting clock cycle access to data for the simulation)**

Regarding claim 17:

The reference discloses The data processing circuit of Claim 15, said logic array emulating at realtime a logic function without logic emulation. **(The Examiner notes paragraph 25 of Hoare which shows that the invention can run at various speeds and even up to faster than real time which reads on this limitation. Paragraph 19, whereby the functional logic simulation is broken up into two parts, the logic based and the timing based. The timing propagation simulation represents non-logic element emulation.))**

Regarding claim 18:

The reference discloses The data processing circuit of Claim 15, said logic array having an internal logic processing cells and peripheral communication cells, the signals of said scheduled times processor controlling the operation of said logic array through at least one of said internal logic processing cells or through at least one of said peripheral communication cells. **(Hoare. Paragraph 64 whereby the simulation engines are peripherally connected to the scheduler, element 110, and host workstation of Figure 1. The engines, scheduler and workstation represent groups of cells of processing and are contained in the modules in the reference)**

Regarding claim 19:

The reference discloses The data processing circuit of Claim 15, the internal logic processing cells and the peripheral communication cells exchanging data through a single group of lines on which is set an exchange per time unit, **(Hoare. Figure 1, element 107 whereby each simulation engine module, communicates through its**

single line group. Further paragraph 42 recites single clock cycle access to a block of stored data.) the cells generating signals relative to random events or scheduled events to said scheduled times processor, said scheduled times processor providing a command group to each of the cells. **(Hoare. The scheduler, element 110, represents the scheduled time processing unit and host workstation of Figure 1 provides a user interface for interaction. The simulation engines, elements 105, deal with the signaling for the events. The command group is represented by the scheduler which allocates events as required by timing)**

Regarding claim 20:

The reference discloses The data processing circuit of Claim 18, said internal logic processing cells processing a logic word per time unit. **(Paragraph 42, recites single clock cycle access to a block of data and its corresponding command, such as read/write, which reads on the logic word per time unit whereby logic words are represented as read/write or other events. This is further stated in paragraph 85 whereby a read/write operation is performed in either a single clock cycle or multiple clock cycles depending on the size of the operation and its corresponding data)**

Regarding claim 21:

The reference discloses The data processing circuit of Claim 20, said internal logic processing cells adapted to merge several data groups issued with serval respective identities and to memorize each merged logic word. **(Paragraph 37 recites that the simulation engine allows for multiple pending events, such as read/writes, to be evaluated within one or more clock cycles. Paragraph 16 recites the storage of data as it is being evaluated for scheduling which reads on the memorizing of a merged logic word in that multiple operations are performed in a single cycle and the operations are based on the scheduler "memorizing" by storing the appropriate event and its relevant data)**

Regarding claim 22:

The reference discloses The data processing circuit of Claim 20, said peripheral communication cells adapted to sample the logic words received and to generate merged logic words. **(Paragraph 37 recites that the**

simulation engine allows for multiple pending event execution. Paragraph 16 recites the storage of data as it is being evaluated for scheduling and further the read/write recitation reads on the communication direction in that a read operation brings data into the scheduled event and the write operation sends the scheduled event data result out.)

Regarding claim 23:

The reference discloses The data processing circuit of Claim 19, said logic array communicating external of the circuit, said logic array setting up memorized logic words adapted to be read or modified. **(Paragraph 16 recites the storage of data as it is being evaluated for scheduling and further the read/write recitation reads on the communication means in that a read operation communicates data into the scheduled event and the write operation communicates the scheduled event data result out.)**

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. All Claims are rejected.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAIF ALHIJA whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300. *Informal or draft communication, please label PROPOSED or DRAFT*, can be additionally sent to the Examiners fax phone number, (571) 273-8635.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

May 18, 2011

/Saif A Alhija/

Examiner, Art Unit 2128